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AN10047

Handheld devices using the ISP1582; ISP1583

Rev. 04 — 20 February 2009 **Application note**

Document information

Info	Content
Keywords	isp1582, isp1583, usb, universal serial bus
Abstract	This is an application note on handheld devices using the ISP1582 or ISP1583.

ST-NXP Wireless

Revision history

Rev	Date	Description
04	20090220	Globally changed NXP Semiconductors and NXP to ST-NXP Wireless. Also updated the legal text.
03	20080121	Third release. Updated Section 2
02	20060906	Second release. Section 2.1: updated the second paragraph.
01	20050301	First release.

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1. Introduction

This document explains the application of handheld devices using the ISP1582 or ISP1583.

2. Power mode

Handheld devices can be powered using either power-sharing mode or bus-powered mode.

The ISP1582 supports bus-powered mode and the ISP1583 supports both bus-powered and power-sharing modes.

2.1 Power-sharing mode

As can be seen in Fig 1, in power-sharing mode, $V_{CC(3V3)}$ is supplied by the output of the 5 V-to-3.3 V voltage regulator. The input to the regulator is from V_{BUS}. $V_{CC(I/O)}$ is supplied through the power source of the system. When the USB cable is plugged in, the ISP1583 goes through the power-on reset cycle. In this mode, OTG is disabled.

In power-sharing mode, it is recommended that you connect pull-up signals to $V_{CC(I/O)}$ instead of $V_{CC(3V3)}$. This is to ensure that when V_{BUS} is lost, interfacing signals are properly handled. Connect RPU to $V_{CC(3V3)}$ through a 1.5 kΩ pull-up resistor.

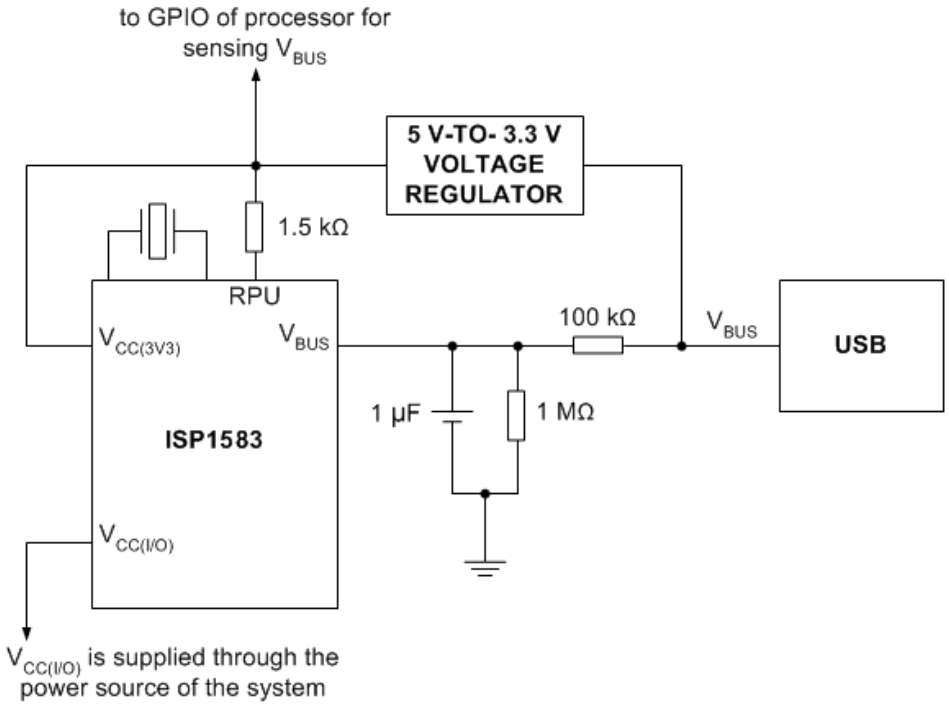

Fig 1. Power-sharing mode

In power-sharing mode, the processor will experience continuous interrupt when V_{BUS} is lost; see Fig 2. This is because the default status of the interrupt pin when operating in sharing mode with V_{BUS} not present is LOW. To overcome this, implement external V_{BUS}

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sensing circuitry. The output from the voltage regulator can be connected to pin GPIO of the processor to qualify the interrupt from the ISP1583.

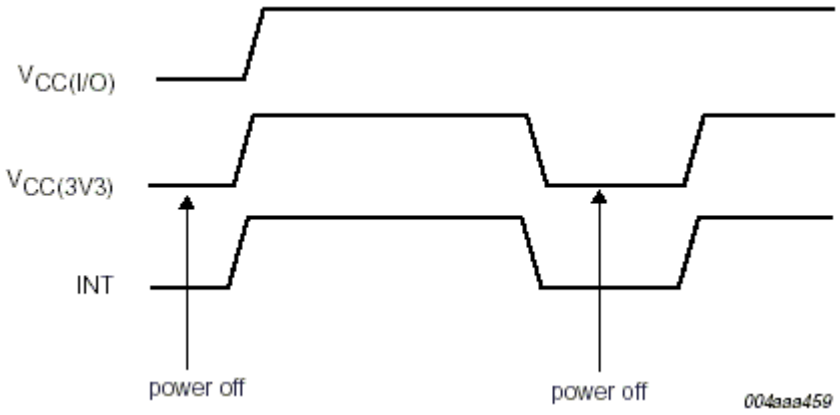

Fig 2. Interrupt pin status during power off in power-sharing mode

2.2 Bus-powered mode

In bus-powered mode, $V_{CC(3V3)}$ and $V_{CC(I/O)}$ are supplied by the output of the 5 V-to-3.3 V voltage regulator; see Fig 3. The input to the regulator is from V_{BUS}. On plugging in the USB cable, the ISP1582/3 goes through the power-on reset cycle. In this mode, OTG is disabled.

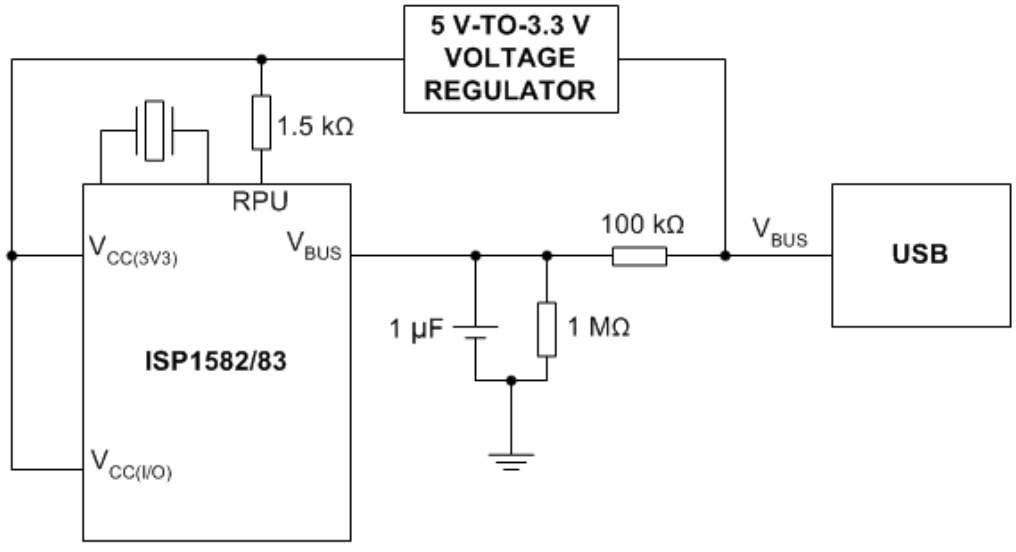

Fig 3. Bus-powered mode

3. Suspending a device

In the following subsections, you will find the recommended sequence to properly suspend the ISP1582/3 to achieve lowest power consumption for various scenarios. This is because most handheld devices are battery operated, and are required to work in lowest power consumption mode when in idle state.

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3.1 Connecting a DC charger to the USB port

Some handheld devices may have battery charging through the USB port. These devices may encounter problems, such as waking up the ISP1582/3 unnecessarily when the DC charger is connected to the USB port. The ISP1582/3 can be woken up from suspend in any of the following ways:

- Activities on the bus
- Wake-up on chip select
- Using the WAKEUP pin
- Presence of V_{BUS}

The following steps can be used to set the ISP1582/3 into suspend mode, if a DC charger is connected to the USB port instead of a USB cable.

1. The device must be in suspend mode. It is recommended, though not necessary, that the device is interrupt driven. The device must have the V_{BUS} present interrupt enabled.
2. On detecting the presence of a V_{BUS} interrupt or the V_{BUS} status bit, issue an unlock command by using the Unlock Device register (7Ch) to unlock the chip. Write unlock code AA37h to the Unlock Device register.
3. Issue a soft reset and enable SoftConnect[1].

   A soft reset is needed if you do not know the previous states of the ISP1582/3. Soft reset can be performed using the Mode register (0Ch). In the Mode register, write logic 1 followed by logic 0 to the SFRESET bit to enable the software initiated reset to the ISP1582/3. The ISP1582/3 must be reinitialized to the default setting.

   If, however, the ISP1582/3 is reset before the DC charger is connected to the USB port, you may just enable the SoftConnect (SOFTCT) bit in the Mode register. Writing logic 1 to bit SOFTCT will enable the connection of the 1.5 kΩ pull-up resistor on pin RPU to the DP line.

   The device is now ready for bus enumeration. Steps 1 to 3 are for the systems that do not know whether V_{BUS} is from a DC charger or a USB cable. This makes the firmware easier to manage.
4. If a DC charger is connected to the USB port, there will be no activity on the bus and the microcontroller will receive a suspend interrupt. After the microcontroller has received the suspend interrupt, the microcontroller can set the ISP1582/3 to sleep mode again. If the connection is using a USB cable, then the device is ready for bus enumeration.
5. If your system has masked off the interrupt and can detect that V_{BUS} is from the DC charger, it is advisable to wait for more than 3 ms. The delay is required for the ISP1582/3 to enter the correct internal state. This is prompted by the ISP1582/3 through the interrupt when the ISP1582/3 is ready for suspend.

3.2 Low-battery situation

When the battery for handheld devices is low while there is communication between the host and peripheral, that is, with the USB cable connected, the ISP1582/3 must be set into suspend mode. The following steps can be performed to suspend the ISP1582/3:

[1] SoftConnect is a trademark of ST-NXP Wireless.

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1. Force the ISP1582/3 into full-speed mode by writing logic 1 to the FORCEFS bit in the Test Mode register (84h).
2. Disable SoftConnect by writing logic 0 to the SOFTCT bit in the Mode register (0Ch).
3. Issue a soft reset to the ISP1582/3 by writing logic 1, followed by logic 0 to the SFRESET bit in the Mode register.
4. Wait for a minimum of 3 ms, before sending the ISP1582/3 back into suspend mode.

4. Device suspend current

Table 1 shows the suspend current measurement of the ISP1582/3 under various conditions.

Table 1. Suspend current measurement

CLKAON	Supply voltage	Test conditions	Core (mA)	I/O (mA)
On	V_{CC} = 3.3 V $V_{CC(IO)}$ = 3.3 V	Suspend with PLL on	19.60	3.48
Off	V_{CC} = 3.3 V $V_{CC(IO)}$ = 3.3 V	Suspend with PLL off; V_{BUS} present; SoftConnect on	0.107	3.48
Off	V_{CC} = 3.3 V $V_{CC(I/O)}$ = 3.3 V	Suspend with PLL off; V_{BUS} present; SoftConnect off	0.105	3.52
Off	V_{CC} = 3.3 V $V_{CC(IO)}$ = 3.3 V	Suspend with PLL off; V_{BUS} not present	0.107	3.50

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